

MP7524 DIE

8-Bit Buffered Multiplying
Digital-to-Analog Converter
CMOS Die Specifications



Micro Power Systems



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PHYSICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V _{DD} to GND	0 V, +17 V
V _{REF} to GND	+25 V
Digital Input Voltage (V _{IN}) to GND	-0.5 to V _{DD} +0.5 V
V _{OUT1} , V _{OUT2} (pin 1, pin 2) to GND	-0.5 V to +6.5 V
T _J (maximum)	150°C

Ordering Information

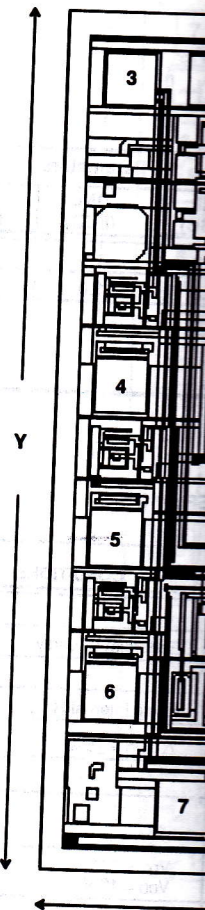
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7524S-DIE	0.5	1.0	2.5
MP7524T-DIE	0.25	1.0	2.5

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V & 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		0.5	LSB	End Point Linearity
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		2.5	LSB	Using Internal R _{FB}
PSRR	Power Supply Rejection Ratio		800 200	ppm / % ppm / %	V _{DD} = 5 V V _{DD} = 15 V
I _{OLKG}	Output Leakage Current		50	nA	
R _{IN}	Input Resistance	5	20	KΩ	
V _{IH}	Logic "1"	2.4 13.5		V V	V _{DD} = 5 V V _{DD} = 15 V
V _{IL}	Logic "0"		0.8 1.5	V V	V _{DD} = 5 V V _{DD} = 15 V
I _{LKG}	Input Leakage Current		1	μA	
I _{DD}	Supply Current		2	mA	Inputs 0 V or V _{DD}

NOTES:

- Die are 100% electrically tested in wafer form to meet the limits shown above.
- Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
- Absolute maximum ratings are for TA = 25°C unless otherwise specified.
- AC electrical characteristics are neither guaranteed nor tested in die form.
- Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
- Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.



Die Data

Die Size	X = 63 mil
Pad Size	4 X 4 m
Pad Metal	
Thickness	15 mil
Backside Material	
Backside Potential	